

## WHAT IS CLAIMED IS:

1. 1. A method of generating a non-integer frequency divided clock signal comprising the steps of:
  3. a) generating a number K of output signal phases P(0) to P(K-1);
  4. b) outputting a present value of an integer index in response to a logic transition of a shift clock signal;
  5. c) selecting one of the K output signal phases P(0) to P(K-1) corresponding to the present value of the integer index as a clock output signal using a glitch free clock selector circuit;
  6. d) clocking a synchronous divide by N counter with the clock output signal generating the non-integer frequency divided clock signal and the shift clock signal;
  7. e) determining when the synchronous divide by N counter has been clocked N times by the clock output signal, wherein the shift clock signal is generated by a transition of the clock output signal following an Nth transition of the clock output signal;
  8. f) receiving an integer fractional divisor having a value less than (K-1); and
  9. g) adding the value of the integer fractional divisor to the present value of the integer index in a modulo (K-1) adding circuit generating a new present value of the integer index.
1. 2. The method of claim 1, wherein the non-integer frequency divided clock signal is used as a feedback clock signal of a phase locked loop circuit having a multiphase voltage controlled oscillator generating the K of equally phased output signals P(0) to P(K-1).

- 1       3.     The method of claim 1, wherein the K output signal phases P(0) to P(K-1)  
2     each have a period T and are progressively phase shifted by an equal amount T/K.

- 1       4. A circuit for generating a non-integer frequency divided clock signal that is  
2 frequency divided from a clock output signal comprising:  
3           a multiple phase clock having a number K of output signal phases P(0) to  
4 P(K-1);  
5           circuitry for outputting a present value M of an integer index in response to a  
6 logic transition of a shift clock signal;  
7           glitch free clock selector circuitry for selecting one of the K output signal  
8 phases P(M) as a clock output signal in response to the present value M of the integer  
9 index;  
10          a synchronous divide by N counter clocked by the clock output signal thereby  
11 generating the frequency divided clock signal and the shift clock signal;  
12          circuitry in the divide by N counter for determining when the divide by N  
13 counter has been clocked N times by the clock output signal, wherein the shift clock  
14 signal is generated by a transition of the clock output signal on a transition following  
15 an Nth transition of the clock output signal;  
16          circuitry for receiving an integer fractional divisor having a value S having a  
17 value less than (K-1); and  
18          modulo (K-1) adding circuitry for adding the value S to a value of the integer  
19 index generating the present value M.

1       5. The circuit of claim 4, wherein the non-integer value is (N+S/K).

1       6. The circuit of claim 4, wherein the glitch free clock selector circuitry  
2 comprises a K to one Phase multiplexer (MUX) receiving the K clock phase signals  
3 and generating a Phase MUX output as P(M), a selected one of the K clock phase  
4 signals, in response to a K bit MUX select signal, wherein only one of the K bits is a  
5 logic one corresponding to the present value M of the integer index.

- 1       7.     The circuit of claim 4, wherein the modulo (K-1) adding circuitry comprises:  
2                   circuitry for converting S to a K bit phase select signal wherein one of the K  
3                   bits is a logic one and K corresponds to the value S;  
4                   a number of K (K to one) Select MUXs, wherein each input of the K Select  
5                   MUXs is coupled to one of the K bits of the K bit MUX select signal and the ordering  
6                   of the coupling for each of the K Select MUXs is rotationally shifted by one from an  
7                   adjacent Select MUX; and  
8                   a K bit register, wherein each register bit stores a state of the output of each of  
9                   the K Select MUXs in response to the shift clock signal and the outputs of the K bit  
10                  register form the K bit MUX select signal.
- 1       8.     The circuit of claim 6, wherein the glitch free clock selector circuitry further  
2                  comprises a logic circuit for generating the clock output signal as a logic combination  
3                  of the Phase MUX output and a sequential gating signal that depends on a previous  
4                  state of the clock output signal.
- 1       9.     The circuit of claim 4, wherein the K output signal phases P(0) to P(K-1) each  
2                  have a period T and are progressively phase shifted by an equal amount T/K.

- 1        10. A phase locked loop circuit for generating a phase clock signal with a  
2 frequency that is a non-integer multiple of a reference clock signal comprising:  
3              a multiphase voltage controlled oscillator (MVCO) generating the phase clock  
4 signal as one of a number K of output signal phases P(0) to P(K-1) and the frequency  
5 of the phase clock signal is controlled by a control voltage;  
6              a phase frequency detector for comparing a frequency divided clock signal to  
7 the reference clock signal and generating a phase/frequency error signal;  
8              circuitry for converting the phase/frequency error signal to the control voltage;  
9 and  
10              division circuitry for generating the frequency divided clock signal by  
11 frequency dividing a selected one P(M) of the K equally phased output signals by a  
12 non-integer value, wherein the division circuitry has circuitry for outputting a present  
13 value M of an integer index in response to a logic transition of a shift clock signal,  
14 glitch free clock selector circuitry for selecting one of the K equally phased output  
15 signals P(M) as a clock output signal in response to the present value M of the integer  
16 index, a synchronous divide by N counter clocked by the clock output signal thereby  
17 generating the frequency divided clock signal and the shift clock signal, circuitry in  
18 the divide by N counter for determining when the divide by N counter has been  
19 clocked N times by the clock output signal, wherein the shift clock signal is generated  
20 by a transition of the clock output signal on a transition following an Nth transition of  
21 the clock output signal, circuitry for receiving an integer fractional divisor having a  
22 value S having a value less than (K-1), and modulo (K-1) adding circuitry for adding  
23 the value S to a value of the integer index generating the present value M.
- 1        11. The phase locked loop circuit of claim 10, wherein the non-integer multiple  
2 has a value (N+S/K).

1       12. The phase locked loop circuit of claim 10, wherein the glitch free clock  
2 selector circuitry comprises a K to one Phase multiplexer (MUX) receiving the K  
3 clock phase signals and generating a Phase MUX output as P(M), a selected one of  
4 the K clock phase signals, in response to a K bit MUX select signal, wherein only one  
5 of the K bits is a logic one corresponding to the present value M of the integer index.

1       13. The phase locked loop circuit of claim 10, wherein the modulo (K-1) adding  
2 circuitry comprises:

3              circuitry for converting S to a K bit phase select signal wherein one of the K  
4 bits is a logic one and K corresponds to the value S;

5              a number of K (K to one) Select MUXs, wherein each input of the K Select  
6 MUXs is coupled to one of the K bits of the K bit MUX select signal and the ordering  
7 of the coupling for each of the K Select MUXs is rotationally shifted by one from an  
8 adjacent Select MUX; and

9              a K bit register, wherein each register bit stores a state of the output of each of  
10 the K Select MUXs in response to the shift clock signal and the outputs of the K bit  
11 register form the K bit MUX select signal.

1       14. The phase locked loop circuit of claim 12, wherein the glitch free clock  
2 selector circuitry further comprises a logic circuit for generating the clock output  
3 signal as a logic combination of the Phase MUX output and a sequential gating signal  
4 that depends on a previous state of the clock output signal.

1       15. The phase locked loop circuit of claim 10, wherein the K output signal phases  
2 P(0) to P(K-1) each have a period T and are progressively phase shifted by an equal  
3 amount T/K.

1        16. A data processing system comprising:

2              a central processing unit (CPU) clocked by a CPU clock signal;

3              a random access memory (RAM);

4              a read only memory (ROM);

5              an I/O adapter;

6              a bus system coupling said CPU to said ROM, said communications adapter,

7              said I/O adapter, and said RAM, wherein the CPU clock signal is generated by phase

8              locked loop circuitry as a non-integer multiple of a reference clock signal, the phase

9              locked loop circuitry having a multiphase voltage controlled oscillator (MVCO)

10             generating the CPU clock signal as one of a number K of output signal phases P(0) to

11             P(K-1) and the frequency of the CPU clock signal is controlled by a control voltage;

12             a phase frequency detector for comparing a frequency divided clock signal to

13             the reference clock signal and generating a phase/frequency error signal;

14             circuitry for converting the phase/frequency error signal to the control voltage;

15             and

16             division circuitry for generating the frequency divided clock signal by

17             frequency dividing a selected one P(M) of the K equally phased output signals by a

18             non-integer value, wherein the division circuitry has circuitry for outputting a present

19             value M of an integer index in response to a logic transition of a shift clock signal,

20             glitch free clock selector circuitry for selecting one of the K equally phased output

21             signals P(M) as a clock output signal in response to the present value M of the integer

22             index, a synchronous divide by N counter clocked by the clock output signal thereby

23             generating the frequency divided clock signal and the shift clock signal, circuitry in

24             the divide by N counter for determining when the divide by N counter has been

25             clocked N times by the clock output signal, wherein the shift clock signal is generated

26             by a transition of the clock output signal on a transition following an Nth transition of

27       the clock output signal, circuitry for receiving an integer fractional divisor having a  
28       value S having a value less than (K-1), and modulo (K-1) adding circuitry for adding  
29       the value S to a value of the integer index generating the present value M.

1       17.      The data processing system of claim 16, wherein the glitch free clock selector  
2       circuitry comprises a K to one Phase multiplexer (MUX) receiving the K clock phase  
3       signals and generating a Phase MUX output as P(M), a selected one of the K clock  
4       phase signals, in response to a K bit MUX select signal, wherein only one of the K  
5       bits is a logic one corresponding to the present value M of the integer index.

1       18.      The data processing system of claim 16, wherein the modulo (K-1) adding  
2       circuitry comprises:

3               circuitry for converting S to a K bit phase select signal wherein one of the K  
4       bits is a logic one and K corresponds to the value S;

5               a number of K (K to one) Select MUXs, wherein each input of the K Select  
6       MUXs is coupled to one of the K bits of the K bit MUX select signal and the ordering  
7       of the coupling for each of the K Select MUXs is rotationally shifted by one from an  
8       adjacent Select MUX; and

9               a K bit register, wherein each register bit stores a state of the output of each of  
10      the K Select MUXs in response to the shift clock signal and the outputs of the K bit  
11      register form the K bit MUX select signal.

1       19.      The data processing system of claim 17, wherein the glitch free clock selector  
2       circuitry further comprises a logic circuit for generating the clock output signal as a  
3       logic combination of the Phase MUX output and a sequential gating signal that  
4       depends on a previous state of the clock output signal.

- 1        20. The data processing system of claim 16, wherein the K output signal phases
- 2         $P(0)$  to  $P(K-1)$  each have a period T and are progressively phase shifted by an equal
- 3        amount  $T/K$ .